AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [002] with the following amended paragraph:

[002] The present application is related to another application, entitled CONNECTION PACKAGE FOR HIGH-SPEED INTEGRATED CIRCUIT, Application No. [[_____]] 09/990,144, filed concurrently on even date, and also assigned to the Assignee of the present invention. The related application is incorporated by reference herein.

Please replace paragraph [030] with the following amended paragraph:

[030] ~~Figure 9 (b) illustrates a simplified diagram~~ Figures **9(b)(1)** and **9(b)(2)** illustrate simplified diagrams of an exemplary via connection for ground connectors from two layers.

Please replace paragraph [037] with the following amended paragraph:

[037] Figure **3 (a)** illustrates a simplified diagram of a partial view of an exemplary single-layer substrate with transmission lines for a high-speed integrated circuit. The high-speed integrated circuit ("IC") 200 is positioned in recess 202 formed typically toward the center of substrate 201. The IC 200 has signal pads 220, 225 at its outer edges. Transmission lines, e.g., microstrips 210, 215, are formed to receive bonding wires from signal pads 220, 225 for transmission to external terminals 230, 235. The microstrips 210, [[214]] 215 are typically identical in size and shape at the inner edges of the substrate 201 near the signal pads 220, 225 (e.g., area 213). For a high-speed signal connected through a GPPO connector, its width at the connector end of 230, 235 should preferably match the width of the conductor core diameter of the GPPO connectors 231, 236. However, such width, at the IC end, will encroach on

neighboring transmission lines, thus limiting the number of transmission lines that can support the signal pads from the IC. However, simply narrowing the width of the transmission line at the IC end will cause impedance discontinuity for the overall transmission path, since a reduction in width results in reduced capacitance to ground, which increases the transmission line's characteristic impedance based on the equation: $Z = 1 / vC$, where Z is impedance, v is velocity of the signals and C is the capacitance per unit length. To maintain impedance continuity for a typical 50-ohm transmission line, the capacitance must be compensated by some other means. In accordance with one embodiment of the present invention, the thickness of the substrate 201 is substantially identical to the width of the dielectric "ring" portion of the cylindrical GPPO connectors 231, 236. This provides a smooth transition between the ground plane at the bottom of the substrate and the ground connection located at the outer cylinder portion of the GPPO connectors. It should be noted that the term "microstrip," "transmission line," ~~"stripeline,"~~ "stripline," or the like is used to describe or claim either a signal path or a power or ground path. It may have various shapes, including, without limitation, lines or no particular patterns (e.g., Figures **12(d)**, **(h)**).

Please replace paragraph [043] with the following amended paragraph:

[043] As can be appreciated by those skilled in the art, for a CLC network, the impedance is determined by: $Z = [[(L/C)]] \sqrt{(L/C)}$, where $C = C_p + C_s$. To maintain the characteristic impedance Z at, say, 50 ohm, as is the case for a high-speed transmission path, with L = 0.170 nH contributed from the bonding wires, the value of C needs to be around 70 fF. If the capacitance C_p from the signal pad is about 35 fF, C_s from the microstrip needs to be 35 fF. To achieve such additional required capacitance, or any required value under different circumstances, the width of a portion 610, 615 of the microstrips can be increased, as shown in Figure **6**, to achieve the desired effective value of 35 fF. The widened portion 610, 615 is located near the signal pads 600, 605 in an area that receives the bonding wires. The size and shape of the portion 610, 615 are typically identical. The precise amount of widening, as well as its extent lengthwise, can be readily computed using the aforementioned microwave design tool.

In Figure **6**, while the portion 610, 615 is rectangularly shaped, it is not limited to that shape and may have other shapes. Also, while portion 610, 516 is symmetrically situated along each of the microstrips, it may not be symmetrical in other embodiments.

Please replace paragraphs [050]-[052] with the following amended paragraphs:

[050] Figure **9 (a)** illustrates a simplified diagram of an exemplary ground connection transitioning from one layer to another layer in accordance with one embodiment of the present invention. From the IC's end, the ground plane 810 is in-between the first layer 801 and the second layer 802. At the external connector's end, the ground plane 830 is at the bottom of the second layer 802. A via connection 815 is made to connect ground 810 to ground 830 through the second layer 802. Such transition is an abrupt transition, which is normally undesirable for high-speed application. To avoid creating a discontinuity at this junction, at least one of the ground via connections is being placed directly underneath the signal microstrip 820 (as further shown in ~~Figure 9 (b)~~ Figures **9(b)(1)** and **9(b)(2)**), so that the return ground current will not take a circuitous path. The microstrip 820 may carry a high-speed signal to be connected to a coaxial connector, or a lower speed signal to be connected to the external lead terminal. If the dimensions of the connector pin and the dielectric ring require three or more layers of separation between 820 and 830, the ground plane transition and line widening process can be repeated.

[051] ~~Figure 9 (b) illustrates a simplified diagram~~ Figures **9(b)(1)** and **9(b)(2)** illustrate simplified diagrams of an exemplary via connection for ground connectors of a multi-layer substrate. Microstrip 910, which may be a high-speed signal or a lower-speed signal, is formed on top of first layer 915 of dielectric material for transmission. First ground plane connection 930, which is formed on top of second layer 920 but below first layer 915, is closer to microstrip 910 than a second ground plane connection 950 is to microstrip 910, thus allowing microstrip 910 to have smaller geometry while it is located above the first ground connection 930. Via connection 940 provides an abrupt transition from first ground plane connection 930 to second ground plane connection 950. Second ground plane connection 950 is formed at the bottom of second layer 920, thus providing a thicker dielectric material underneath microstrip 910.

[052] As can be appreciated by those skilled in the art, because of the different distances (i.e., thickness) between ground connections 930, 950, and microstrip 910, the width of microstrip 910 needs to be widened to maintain a constant impedance structure, i.e., tapering out as the ground plane is further away. Such tapering out of microstrip width, from the IC's end to the connector's end, makes dimensional transformation more achievable and with better results. ~~The second drawing in~~ Figure 9(b)(2) shows a top-down view of an exemplary tapering structure of microstrip 910. Microstrip 910 is narrow over the ground plane connection 930 and wider over the ground plane connection 950. The tapering occurs over the via connection 940. Although a substrate of only two layers is illustrated, it should be apparent to those skilled in the art that additional layers may be implemented to take advantage of the variable ground plane approach. While Figures 9 (a), ~~and 9 (b)~~ 9(b)(1) and 9(b)(2) have been illustrated using ground plane connections, similar illustrations can be shown using power plane connections if the signal ground has non-zero DC potential.

Please replace paragraph [066] with the following amended paragraph:

[066] Figures **12 (c), (d), (e), (f)** continue to illustrate Layers 3, 4, 5, 6, where signals 121, 122 continue to be routed through what has become a "coaxial" connector – conducting via in the middle, surrounded by dielectric material within a circle and bounded by ground planes' circular openings. The ratio of the diameter of the via for the signal to the diameter of the ground opening follows the formula for coaxial cables: $Z = 60 \log (b/a) / [\eta \times \varepsilon]$ ~~[η x ε]~~ where "Z" is the desired impedance, "b" is the diameter of the opening, "a" is the diameter of the via, "ε" is the dielectric constant of the dielectric layer, and "η" is the efficiency of the capacitance between the ground openings to the center via as compared to that in a real coax cable of the same dimensions. "η" of course depends on layer thickness, "ε" and "b". It is typically in the order of 80%. Note that ground plane 125 has taken on different patterns from layer to layer. The pattern of the ground plane (except for the diameter of the openings) does not affect the impedance calculation described above, as most of the capacitance is between the edge of the opening and the center via for signal.